substrate so as to be in electrical contact with the surface of said first layer coincident with the surface of said substrate at each cell in said array, and

a spacer layer of insulating material insulating said word line contact from said bit line contact.

Please add a new claim 4 as follows:

4. The apparatus of claim 3 wherein said bit line contact contacts said first layer at all points between said spacer layers of the word line contacts of adjacent memory cells.

Please add a new claim 5 as follows:

5. The apparatus of claim 3 wherein said bit line contact contacts said first layer at at least some points between said spacer layers of the word line contacts of adjacent memory cells and runs over the top of said word line and is insulated therefrom by said spacer layer.

Remarks

REMARKS

The specification and drawings have been corrected as suggested by the Examiner, and the spelling error in claim 1 has been corrected.

In response to the rejection of claim 1 under 35 U.S.C. §112 for indefiniteness, the second element of claim 1 has been amended as follows to eliminate the ambiguity regarding use of the word "intersecting":

a vertical MOS transistor formed by alternating N-type and P-

type doped layers in said substrate [intersecting] and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layer surround said well,

Also, use of the word "materials" has been deleted and "layers" has been substituted

As to the Section 112 rejection of claim 2, the following amendments have been made to clarify the relationship between the conductivity types:

a semiconductor substrate of a first conductivity type having a surface suitable to act as a drain region of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel [region] of a vertical MOS transistor formed in said substrate;

Also, the following amendments have been made to change the structure of the claim for better clarity and to clarify that the first conductivity type mentioned on lines 9-9 of the is the same conductivity type as the first conductivity type mentioned mentioned for the drain region.

a [first] source region of said semiconductor substrate [between said buried layer and said surface of said substrate, and a second region of said semiconductor substrate] below said buried layer, [both said first and second regions] source region being doped so as to have [a] said first conductivity type;

[a first layer of insulating material covering said surface of said substrate;]

The following changes were made to make the claim more clear and conform the

terminology to the terminology changes made in the other parts of claim 2:

a recessed gate window in the form of a well etched in said semiconductor substrate through said first layer of insulating material, said well being deep enough to penetrate through said [buried layer] channel region and into said source region such that at least some portion of the side wall or sidewalls of said trench are bordered by said source, drain and channel regions [recessed gate window intersect said buried layer and said first and second regions of said semiconductor substrate];

The following changes have been made in response to the prior art rejection:

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well; [with]

The following change was made simply to break the insulating layer covering the floating gate out as a separate element:

an insulating layer formed over said self aligned floating gate [conductive material] so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said [intersection of said well with said buried layer] channel region;

The following change was made to alter the language of the word line clause to eliminate reference to the first insulating layer:

a word line comprising conductive material deposited [on said first insulating layer] so as to extend into said well far enough to overlie at least a portion of said floating gate; and

A change to the preamble has been made to convert the claim to a claim for an array as opposed to a single cell.

The following change has been made to overcome the prior art rejection:

> a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at each said memory cell but insulated from said word line by said second layer of insulating material[, and deposited in a contact window formed in said first insulating layer so as to be in electrical contact with said first region, said first region acting as a drain of said vertical MOS transitor].

Claims 1 and 2 have been rejected under Section 102 or 103 over Mori. In response to this rejection, the claims have been amended to specify that the structures claimed have self aligned floating gates that do not extend beyond the edges of the well. Mori's floating gate is formed using a masking step such that the floating gate material extends up and out of the well over overlies a portion of the surface of the substrate. Although the drawing of Figure 1a shows the edges of the floating gate even with the edges of the well, those skilled in the art appreciate that this floating gate is not self aligned and is formed by a mask (See Col. 9, Lines 28-29 where the poly 1 layer for the floating gates is stated to be "patterned and etched to define the floating gate"). This means that, because of alignment errors and the spacing rules of the design rules, it is not acually possible to prevent some horizontal portions of the floating gate material from extending out past the edges of the well. This means the individual cells of the memory aray cannot be spaced as closely together even in the contactless array. This is because the design rules will require some safety margin in the spacing to make sure that an alignment error does not result in a portion of a floating gate from one cell from

getting too close to or overlapping the well of another cell. This hit to the density of the array is made even worse in the "contacted" array where a bit line contact window to the drain region must be formed at the location of each cell. Such a contact window at each cell requires a separate mask and the design rules will require safety margin spacing between the edge of the well and the edge of the contact window as well as spacing between the opposite edge of the cotact window and the well of the adjacent cell. Further, to make a contacted array as shown in Figure 2b of Mori, the drain region 54 must be brought to the surface and form an area on the surface which is large enough for the contact window to be formed. The design rules will require this contact window area 56 be large enough to encompass the contact window. The design rules will also require a spacing between the edge of the drain region window area 56 and the next cell so that the drain area of one cell does not encroach too closely to or overlap the well of an adjacent cell. This severly degrades the density of the array, and Mori admits this at Col. 5, lines 19-27 where it is stated that, while the contactless array cell size might be 10 square microns, the full contact array with a contact to every cell will have a typical cell size 10 times larger or 100 square microns.

In contrast, no mask is used to define the floating gate because an etch is used which removes all horizontal portions of the poly layer that is deposited into the well after the gate oxide is formed therein. This removes all the horizontal portions of the floating gate material on the surface of the substrate and in the bottom of the well thereby self aligning it with the edges of the well. Thus greater density can be achieved in the structure claimed in claims 1 and 2 than can be achieved in the Mori structure by virtue of the the self aligned floating gates.

With regard to the following change in claim 2:

a second layer of insulating material formed [over] so as to insulate at least a portion of said word line; and

a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at each said memory cell but insulated from said word line by said second layer of insulating material

the language about the coverage by the second layer of insulating material has been changed. The reason for this change is that it is possible that insteady of running the bit line over the top of each cell and its word line, it is also within the genus of the invention to have serpentine bit lines that slalom or wind in and out between the wells just making contact with the exposed drain regions between wells without going over the top of each well in a straight line.

not in spec?

A new claim 3 has been added which includes both a self aligned floating gate and a bit line which runs on the surface of the substrate so as to contact the first layer (drain contact) of each cell in the array. This bit line is much bigger in cross sectional area than the buried layer bit line 24 of the contactless array shown in Figures 1a and 1b. Mori admits at Col. 8, lines 53 et seq. that the trench "cross-sectional area", sic. width, must be cooperatively chosen with the widths of the source and drain bitlines so that after trench formation, the source and drain bit lines form a continuous conductive path around each trench. To maintain as high a density as possible, the amount of excess width of the bitline must be minimized. This means, in the contactless array, the bit line will have very narrow portions (shown at 24 in Figure 1b) running around each trench which will add resistance to the bit line at the location of each trench. This substantially slows down access time by cause RC time constants which are longer in

charging parasitic capacitances coupled to the bit line. Mori admits this at Col. 5, lines 19-24 as a disadvantage of the contactless array. In contrast, the array of new claim 3 will not have this disadvantage and still will have greater density because of the self aligned gates and the fact that contact windows need not be formed to the drain regions for the bit lines as the entire area of the drain regions is open at the surface of the substrate between the insulating spacers that insulate the sides of the word line, as best seen in the cross section of a completed array shown in Figure 33.

All claims are believed to be in condition for allowance, and favorable action is ernestly solicited.

Respectfully submitted,

Dated: November 15, 1997

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(Date of Deposit)

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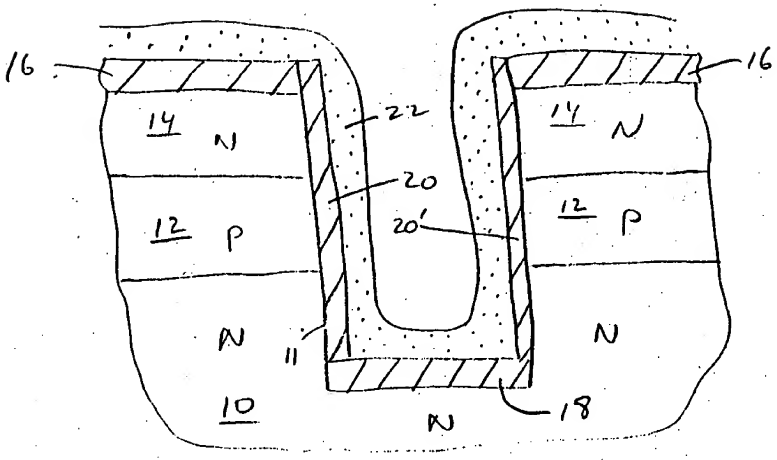


FIG. 1

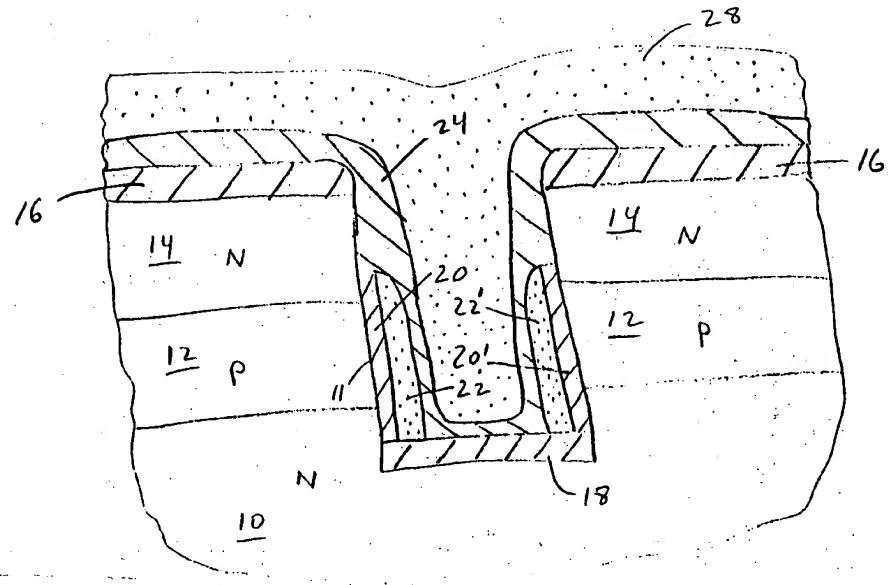
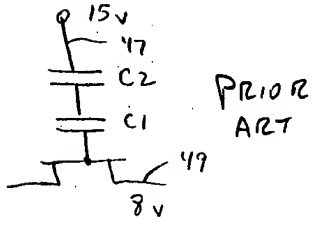
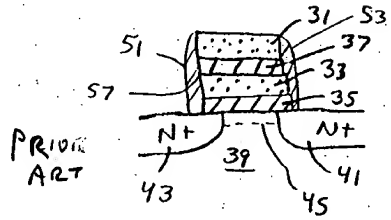


FIG. 2



PRIOR ART

FIG. 3



PRIOR ART

FIG. 4